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10/702,410	11/06/2003	David F. Hepner	SJ0920030018US1	8341

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EXAMINER	
STOYNOV, STEFAN	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/702,410	HEPNER ET AL.	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/06/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

Claims 15 and 22 are objected to because of the following informalities:

Claim 15, line 1, recites "the apparatus" of claim 14, whereas the subject matter of claim 14 corresponds to an article of manufacture comprising a program storage medium.

The dependency of claim 22 appears to be mistaken. For the purpose of examination, it is assumed that claim 22 depends on claim 14 instead of claim 13.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim14-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 14 recites the limitation "system control module" in line 14. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramamurthy et al. US Patent No. 5,758,171 in view of Iwazaki, US Patent No. 6,073,244.

Re claim 1, Ramamurthy discloses an apparatus for regulating power allocated to components within a computer system, the apparatus comprising:

a first sensor configured to sense power drawn by a first device within a computer system

[Ramamurthy does not specifically state a first sensor configured to sense power drawn by a first device within a computer system. However, Ramamurthy discloses the power control circuit (Fig. 1A,1B, and 2, 140, Fig. 3, 340) monitoring (sensing) different power and temperature parameters associated with the PCMCI/PC card (Fig. 1A-3, 110) (column 2, lines 24-40, lines 63-67, column 4, lines 50-52, column 5, lines 24-27). Thus, Ramamurthy inherently discloses a first sensor configured to sense power drawn by a first device within a computer system].

a first power-monitoring module in communication with the first sensor to monitor the power drawn of the first device (column 2, lines 24-40, lines 63-67, column 4, lines 50-52, column 5, lines 24-27, column 6, lines 57-59, Fig. 1A-2, 140, Fig. 3, 340); and

a system control module configured to regulate power allocated to the first device in response to the determination of the power drawn by the first power-monitoring module (column 4, lines 55-63, column 5, lines 59-62, Fig. 3, 330).

Ramamurthy fails to disclose the first device having first device resources needed to satisfy functional demand required of the first device, a first power-monitoring module configured to monitor the functional demand required, and optimizing use of the first device recourses in response to the functional demand.

Iwazaki teaches a clock control apparatus for switching clock frequencies and selectively providing clocks to a plurality of peripheral units according to the states of the peripheral processing units (column 1, lines 6-11). Iwazaki further teaches reducing the power consumption by controlling clock frequencies supplied to the peripheral processing units in response to the processing load states of the peripheral processing units (column 2, lines 56-61, column 3, lines 9-13). Thus, Iwazaki teaches monitoring different processing load states (with corresponding clock frequencies, i.e. functional demand) for the peripheral processing units. In Iwazaki, the apparatus is used for dynamically adjusting the clock frequencies (i.e. changing the peripheral's recourses) according to the processing load associated with each peripheral processing unit (column 6, line 52 – column 6, line 4, FIG. 3). Thus, optimization according to the load

processing state (column 7, lines 9-13) and reduction of power is achieved without compromising performance (column 7, lines 18-32).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the apparatus and the process of monitoring the load states for different peripheral processing units, and dynamically adjusting the peripheral's recourses, as suggested by Iwazaki with the apparatus disclosed by Ramamurthy in order to implement the first device having first device resources needed to satisfy functional demand required of the first device, a first power-monitoring module configured to monitor the functional demand required, and optimizing use of the first device recourses in response to the functional demand. One of ordinary skill in the art would be motivated to do so in order to achieve recourse optimization and power reduction according to the load processing state of the peripheral without compromising processing power.

Re claim 2, Ramamurthy and Iwazaki further disclose the apparatus, further comprising a second sensor configured to sense power drawn by a second device within the computer system (Ramamurthy, column 2, lines 27-28 – two PCMCI/PC cards connected to the adapter card; Iwazaki, FIG(s) 1, 4-8, PERIPHERAL PROCESSING UNIT 31 and 32), the second device having second resources needed to satisfy functional demand required of the second device (Iwazaki, column 6, line 52 – column 7, line 4 – dynamic optimization for the clock/recourse corresponding to second peripheral processing unit (FIG. 4, 32) based on the load processing demand for that peripheral), the system control module further configured to regulate power to the

second device at least partially in accordance with a parameter of the first device (Iwazaki, FIG. 4 – the CLOCK CONTROL CIRCUIT 4 selectively changes the clock frequencies based on peripheral activity/peripheral's processing load states on a common bus 5, detected by BUS ACCESS MONITORING UNIT 44 where the clock frequency for each peripheral is adjusted for that state (column 6, line 52 – column 7, line 4). Thus, the common bus is loaded simultaneously by different peripherals loading the bus differently, and the power regulation is based on adjusting the clock frequencies for both peripherals (column 8, lines 52-52)).

Re claim 3, Iwazaki further teaches the apparatus of claim 2, wherein the system control module is further configured to adjust the power levels in the first and the second devices in accordance with multiple dependent thresholds determined by the respective functional demands of the first and second devices (column 6, line 52 – column 7, line 13, column 8, lines 52-58, FIG. 3).

Re claim 4, Iwazaki further teaches the apparatus of claim 2, wherein the parameter of the first device comprises the functional demand of the device (column 7, lines 18-23).

Re claim 5, Ramamurthy further teaches the apparatus, wherein the system control module is further configured to receive an indication of the temperature of the first device and regulate power of the device in accordance with the indication of temperature and at least one other parameter (column 4, lines 55-63, column 5, lines 59-62, Fig. 3, 330).

Re claim 6, Ramamurthy and Iwazaki further disclose the apparatus of claim 5, wherein the system control module is configured to examine parameters of the first device including temperature, power (Ramamurthy, column 4, lines 55-63, column 5, lines 59-62, column 6, lines 57-59, Fig. 3, 330), and functional demand (Iwazaki, column 8, lines 52-58); to determine a malfunction of the first device in response to the examination of the parameters; and to reduce power transmitted to the first device in response to the determination of malfunction (Ramamurthy, column 2, lines 31-40, lines 59-67, column 4, lines 55-63, column 5, lines 24-27, lines 59-67, Fig. 3, 330).

Re claim 7, Iwazaki further teaches the apparatus of claim 2, wherein the first and second device recourses include at least one of a processor, a memory device, and a device clock (FIG. 1, 1).

Re claim 8, Iwazaki further teaches the apparatus, wherein the functional demand is selected from the group consisting of a number of operations performed, a frequency of operations performed, a peak value of operations performed, a data transfer rate, and a cache hit ratio (column 6, lines 52-59).

Re claim 9, Ramamurthy further discloses the apparatus of claim 2, wherein the first and the second devices are selected from the group consisting of PCI expansion cards, ISA expansion cards, expansion cards connected to a high-speed bus, onboard devices on a motherboard, and a combination thereof (column 1, lines 44-46, column 6, lines 5-6, Fig. 3, 150).

Re claim 10, Ramamurthy further discloses the apparatus of claim 2, wherein at least one of the power-monitoring module and the system control module is located in a

location selected from the group consisting of on an expansion card, independent from an expansion card, on a motherboard, and on a device connected to an expansion card (Fig. 3, system management module PCMCI/PC ADAPTER 330 separate from expansion card PCMCI/PC CARD 110).

Re claim 11, Iwazaki further teaches the apparatus of claim 2, wherein the system control module is configured to control the first and second devices by at least one action selected from the group consisting of shutting off power when functional demand drops below a specified threshold, decreasing the clock speed of selected components when functional demand decreases, increasing the clock speed of selected components when functional demand increases, introducing wait states into logic when functional demand decreases, increasing supplied power when functional demand increases, and decreasing supplied power when functional demand decreases (column 8, lines 52-58).

Re clam 12, Ramamurthy further discloses the apparatus of claim 2, wherein the system control module is further configured to maintain total power consumption of the first and the second devices below a selected level (column 2, lines 24-31).

Re claim 13, Ramamurthy further discloses the apparatus of claim 2, wherein at least one of the power-monitoring module and the system control module include functionality provided by modules selected from the group consisting of hardware, software, kernel extensions, drivers, and embedded operating system (column 4, line 49 – column 5, line 17).

Re claim 14, Ramamurthy discloses an article of manufacture comprising a program storage medium readable by a processor and embodying one or more instructions executable by a processor to perform steps of a method for regulating power allocated to components within a computer system, the method comprising:

sensing power drawn by a first device within a computer system

[Ramamurthy does not specifically state sensing power drawn by a first device within a computer system. However, Ramamurthy discloses the power control circuit (Fig. 1A,1B, and 2, 140, Fig. 3, 340) monitoring (sensing) different power and temperature parameters associated with the PCMCI/PC card (Fig. 1A-3, 110) (column 2, lines 24-40, lines 63-67, column 4, lines 50-52, column 5, lines 24-27). Thus, Ramamurthy inherently discloses sensing power drawn by a first device within a computer system].

monitoring the power drawn required of the first device (column 2, lines 24-40, lines 63-67, column 4, lines 50-52, column 5, lines 24-27, column 6, lines 57-59, Fig. 1A-2, 140, Fig. 3, 340); and

regulating the power allocated to the first device (column 4, lines 55-63, column 5, lines 59-62, Fig. 3, 330)

sensing power drawn by a second device within the computer system (column 2, lines 27-28 – two PCMCI/PC cards connected to the adapter card), the system control module further configured to regulate power to the second device (column 4, lines 55-63, column 5, lines 59-62, Fig. 3, 330, column 2, lines 27-28).

Ramamurthy fails to disclose the first device having first device recourses needed to satisfy functional demand required of the first device, monitoring the functional demand required of the first device, optimizing uses of the first device recourses in accordance with the functional demand of the first device, the second device having second device recourses needed to satisfy functional demand required of the second device, and to regulate power to the second device at least partially in accordance with a parameter of the first device.

Iwazaki teaches a clock control apparatus for switching clock frequencies and selectively providing clocks to a plurality of peripheral units according to the states of the peripheral processing units (column 1, lines 6-11). Iwazaki further teaches reducing the power consumption by controlling clock frequencies supplied to the peripheral processing units in response to the processing load states of the peripheral processing units (column 2, lines 56-61, column 3, lines 9-13). Thus, Iwazaki teaches monitoring different processing load states (with corresponding clock frequencies, i.e. functional demand) for the peripheral processing units. In addition, Iwazaki teaches dynamic optimization for the clock/recourse corresponding to second peripheral processing unit (FIG. 4, 32) based on the load processing demand for that peripheral (column 6, line 52 – column 7, line 4) and selectively changing the clock frequencies based on peripheral activity/peripheral's processing load states on a common bus (FIG. 4, bus 5) detected by a monitoring unit (FIG. 4, BUS ACCESS MONITORING UNIT 44) where the clock frequency for each peripheral is adjusted for that state (column 6, line 52 – column 7, line 4). Thus, the common bus is loaded simultaneously by different peripherals loading

the bus differently, and the power regulation is based on adjusting the clock frequencies for both peripherals (column 8, lines 52-52). In Iwazaki, the apparatus is used for dynamically adjusting the clock frequencies (i.e. changing the peripheral's recourses) according to the processing load associated with each peripheral processing unit (column 6, line 52 – column 6, line 4, FIG. 3). Thus, optimization according to the load processing state (column 7, lines 9-13) and reduction of power is achieved without compromising performance (column 7, lines 18-32).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the apparatus and the process of monitoring the load states for different peripheral processing units loading a common bus, and dynamically adjusting the peripheral's recourses, as suggested by Iwazaki with the article of manufacture disclosed by Ramamurthy in order to implement the first device having first device recourses needed to satisfy functional demand required of the first device, monitoring the functional demand required of the first device, optimizing uses of the first device recourses in accordance with the functional demand of the first device, the second device having second device recourses needed to satisfy functional demand required of the second device, and to regulate power to the second device at least partially in accordance with a parameter of the first device. One of ordinary skill in the art would be motivated to do so in order to achieve recourse optimization and power reduction according to the load processing state of the peripheral without compromising processing power.

Re claim 15, Iwazaki further teaches the article of manufacture, further comprising adjusting the power levels in the first and the second devices in accordance with multiple dependent thresholds determined by the respective functional demands of the first and second devices (column 6, line 52 – column 7, line 13, column 8, lines 52-58, FIG. 3).

Re claim 16, Iwazaki further teaches the article of manufacture, wherein the method further comprises regulating power allocated to the second device by optimizing use of the second device resources in accordance with the functional demand of the second device (column 7, lines 9-13, lines 18-23, column 8, lines 52-58).

Re claim 17, Iwazaki further teaches the article of manufacture, wherein the first and second device resources include at least one of a processor, a memory device, and a device clock (FIG. 1, 1).

Re claim 18, Ramamurthy further discloses the article of manufacture, wherein the first and the second devices are selected from the group consisting of PCI expansion cards, ISA expansion cards, expansion cards connected to a high-speed bus, onboard devices on a motherboard, and a combination thereof (column 1, lines 44-46, column 6, lines 5-6, Fig. 3, 150).

Re claim 19, Ramamurthy further discloses the article of manufacture, wherein monitoring and regulating are performed on at least one component selected from the group consisting of an expansion card, hardware independent of an expansion card, a motherboard, on a device connected to an expansion card, and a combination thereof

(Fig. 3, system management module PCMCI/PC ADAPTER 330 separate from expansion card PCMCI/PC CARD 110).

Re claim 20, Ramamurthy and Iwazaki further disclose the article of manufacture, wherein regulating further comprises at least one action selected from the group consisting of shutting power off (Ramamurthy, column 2, lines 37-40, lines 59-63, column 5, lines 59-62) when functional demand drops bellow a specified threshold (Iwazaki, column 7, lines 18-23, column 8, lines 52-58, FIG. 3), increasing supplied power when functional demand increases, and decreasing supplied power when functional demand decreases.

Re claim 21, Ramamurthy further discloses the article of manufacture, wherein regulating further comprises maintaining total power consumption of the first and the second devices below a specified level (column 2, lines 24-31).

Re claim 22, Iwazaki further teaches the article of manufacture, wherein optimizing comprises at least one action selected from the group consisting of decreasing the clock speed of selected components when functional demand decreases, increasing the clock speed of selected components when functional demand increases, and introducing wait states into logic when functional demand decreases (column 7, lines 9-13, column 8, lines 52-58).

Re claim 23, Ramamurthy discloses a system for regulating power allocated to components within a computer system, the system comprising:

a computer system comprising a processor (Fig. 3, 320), main memory (column 1, lines 6-10, column 6, line 66 – column 7, line 4 – inherently discloses main memory

because the invention regulates power of PCMCI/PC cards in portable computers e.g. laptops, notebooks, etc. These computer systems include main memory), a local bus (column 4, lines 6-7, Fig. 3, 280), and an expansion bus for receiving expansion cards (column 1, lines 44-46, column 6, lines 5-6, Fig. 3, 150);

a first sensor configured to sense power drawn by a first expansion card operably connected to the expansion bus

[Ramamurthy does not specifically state a first sensor configured to sense power drawn by a first expansion card operably connected to the expansion bus. However, Ramamurthy discloses the power control circuit (Fig. 1A,1B, and 2, 140, Fig. 3, 340) monitoring (sensing) different power and temperature parameters associated with the PCMCI/PC card (Fig. 1A-3, 110) connected on the PCI bus (Fig. 3, 150) (column 2, lines 24-40, lines 63-67, column 4, lines 50-52, column 5, lines 24-27). Thus, Ramamurthy inherently discloses a first sensor configured to sense power drawn by a first expansion card operably connected to the expansion bus].

a second sensor configured to sense power drawn by a second expansion card connected to the expansion bus (column 2, lines 27-28 – two PCMCI/PC cards connected to the adapter card); and

a system control module communicating with the first sensor and the second sensor and configured to regulate power allocated to the first expansion card and to regulate power allocated to the second expansion card (column 4, lines 55-63, column 5, lines 59-62, Fig. 3, 330, column 2, lines 27-28).

Ramamurthy fails to disclose the first expansion card having first recourses needed to satisfy functional demand required of the first expansion card, the second expansion card having second recourses needed to satisfy functional demand required of the second expansion card, optimize use of the first resources in accordance with the functional demand of the first expansion card, and regulate power in accordance with multiple dependent thresholds determined by the respective functional demands of the first and second devices.

Iwazaki teaches a clock control apparatus for switching clock frequencies and selectively providing clocks to a plurality of peripheral units according to the states of the peripheral processing units (column 1, lines 6-11). Iwazaki further teaches reducing the power consumption by controlling clock frequencies supplied to the peripheral processing units in response to the processing load states of the peripheral processing units (column 2, lines 56-61, column 3, lines 9-13). Thus, Iwazaki teaches monitoring different processing load states (with corresponding clock frequencies, i.e. functional demand) for the peripheral processing units. In addition, Iwazaki teaches dynamic optimization for the clock/recourse corresponding to second peripheral processing unit (FIG. 4, 32) based on the load processing demand for that peripheral (column 6, line 52 – column 7, line 4) and selectively changing the clock frequencies based on peripheral activity/peripheral's processing load states on a common bus (FIG. 4, bus 5) detected by a monitoring unit (FIG. 4, BUS ACCESS MONITORING UNIT 44) where the clock frequency for each peripheral is adjusted for that state (column 6, line 52 – column 7, line 4). Thus, the common bus is loaded simultaneously by different peripherals loading

the bus differently, and the power regulation is based on adjusting the clock frequencies for both peripherals according to multiple load thresholds (column 8, lines 52-52, FIG. 3, NUM1, NUM2). In Iwazaki, the apparatus is used for dynamically adjusting the clock frequencies (i.e. changing the peripheral's recourses) according to the processing load associated with each peripheral processing unit (column 6, line 52 – column 6, line 4, FIG. 3). Thus, optimization according to the load processing state (column 7, lines 9-13) and reduction of power is achieved without compromising performance (column 7, lines 18-32).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the apparatus and the process of monitoring the load states for different peripheral processing units loading a common bus, and dynamically adjusting the peripheral's recourses according to multiple load thresholds, as suggested by Iwazaki with the system discloses by Ramamurthy in order to implement the first expansion card having first recourses needed to satisfy functional demand required of the first expansion card, the second expansion card having second recourses needed to satisfy functional demand required of the second expansion card, optimize use of the first resources in accordance with the functional demand of the first expansion card, and regulate power in accordance with multiple dependent thresholds determined by the respective functional demands of the first and second devices. One of ordinary skill in the art would be motivated to do so in order to achieve recourse optimization and power reduction according to the load processing state of the peripheral without compromising processing power.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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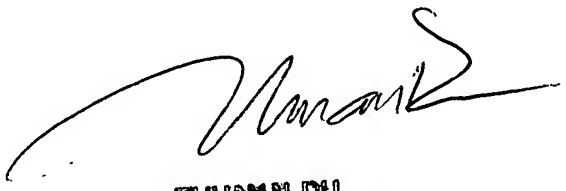

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PRIMARY EXAMINER